Composite clock including a Cs clock, a H-maser clock and a VCO.

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1 Abstract

This article presents the project of creating a composite clock, the advances in its realization and the technical choices. The goal is to generate an output signal which combines the advantages of each clock, the long-term stability for the cesium clock, the mid-term stability for the hydrogen maser clock and short-term stability for the VCO. The control system must keep the stability of the best clock within each duration range. This system is designed for reaching a relative instability of some 10^{-14} *@ 1 s,* 10^{-15} *@* 10^{3} *s and* 10^{-14} *@* 10^{6} *s at 100MHz, depending on the stability of the master clocks.*

2 Introduction

To create this composite clock we wish to control a VCO by a maser clock and a cesium clock (fig. 1). In this project we distinguish 3 technical parts: the Dual Mixer Time Difference (DMTD) system used for estimating the frequency deviation of each standard clock, the digital processing generating a correction signal for the VCO, and the digital to analog conversion which command the VCO (fig. 1). In this paper we will describe the 3 technical parts with their principles and results. The architecture of the system is described on figure 1. The whole system works at 100 MHz which imposes the presence of many frequency multipliers. Moreover we wish to have three outputs, one at 5 MHz, one at 10 MHz and another one at 100 MHz. The shifted oscillator frequency is 100 001 kHz in order to obtain a beat frequency of 1KHz in DMTD output. We use a FPGA and a PC for the digital processing. The FPGA measures the period of the signals which come from the DMTD and it improves these measurements with the appropriate processing.

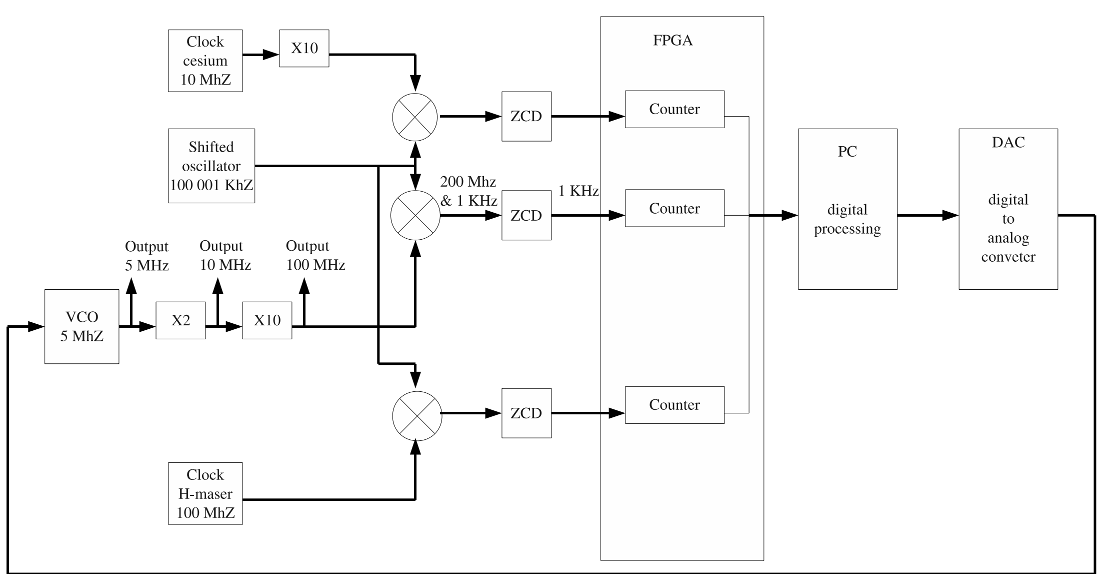

Figure 1: General diagram

The correction to be applied to the VCO is generated by an algorithm running on the PC. The last step is the digital to analog conversion which controls the VCO. We describe the oversampling process that we use with the 16 bits Digital to Analog Converter (DAC).

3 Dual Mixer Time Difference (DMTD)

3.1 Principle

The DMTD system [1] is used to perform 3 comparisons. We compare each standard clock to the same shifted oscillator in order to generate 3 beat frequencies at 1 KHz which inform us about the frequency deviation of each clock. Thus in this system we need a second oscillator: the shifted oscillator. 2 reasons impose this choice: firstly, without this second oscillator, we should shift the VCO frequency and we should have output signals at 5.00005 MHz ,10.0001 MHz and 100.001MHz. Secondly, the noise of the cesium is too high to obtain an information for the short term. The cesium comparison can be used only for the long term. For the short term we need a comparison between 2 oscillators. Each mixer receives 2 signals: one at 100.001 MHz which comes from the shifted oscillator and another one at 100 MHz which comes from one of the standard clocks. The mixer output signal is composed of two components: the frequency sum at 200 MHz and the frequency difference at 1 kHz. Each of these three signals informs us about the frequency deviation of each clock because they were compared with the same oscillator. Then each signal which comes from the mixers is sent to a Zero Crossing Detector.

3.2 The ZCD

Each ZCD [2] has 2 roles. Firstly, the ZCDs eliminate the component at $2\omega_0$ with the first stage of the ZCDs: the low pass filter (fig. 2). Secondly, the ZCDs transform the sine signal of 1 kHz into a square signal of 1 kHz with a very sharp rising edge, and a minimum noise. We must increase the sharpness of rising edges and keep the noise as low as possible. We must find the best compromise between the highest gain and the lowest noise possible. We use four stages to increase the slope of the signals. The four stages after the first one are composed of a high gain and a low pass filter for the first two amplifier stages. The high gain allows to increase the signal slope and the low pass filter allows to decrease the bandwidth, therefore the noise. Only the first 2 amplifier stages have a low pass filter because the noise spectrum density equivalent for the four amplication stages depends mainly on the first amplifier stage.

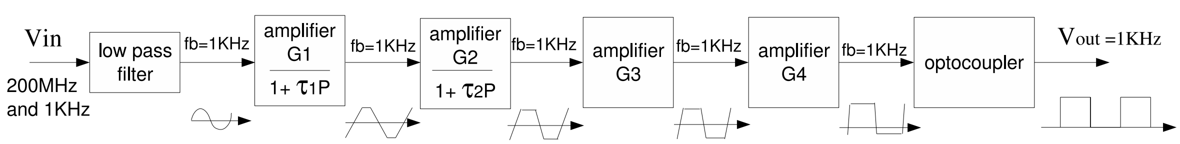

Figure 2: ZCD diagram.

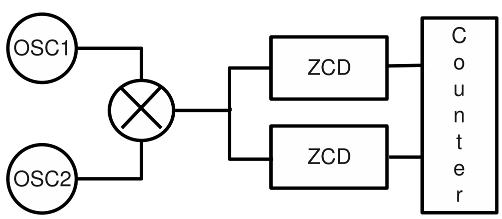

Figure 3: diagram of test

3.3 Test

In order to test the ZCDs, we generate a beat frequency, we split it and send it into 2 ZCDs and thanks to a counter we measure the time difference between the rising edges of these 2 ZCDs (fig.3). The time difference between the 2 ZCDs is not important but the time stability and the jitter are significant. We can see the result on figure 4 (grey curve). After about 3 days of measurement we note that the ZCDs need a heating time of about 1 day. This heating time is due to 8 cm of polystyrene which covers the ZCDs. The measured jitter is about 3.5 ns peak to peak, with a standard deviation $\sigma = 5.5 \times 10^{-10}s$ after the heating time.

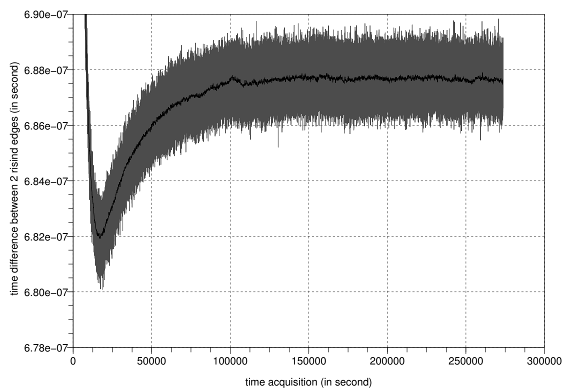

Figure 4: result of test 1.

Even if the ZCDs are covered in polystyrene, we conclude after many tests that the ZCDs are sensitive to the temperature variations [3]. It is not visible on figure 4, but when we trace the modified Allan deviation of this measurement without the heating time, we observe that this signal is composed of 2 noises: a white phase noise and a Flicker phase noise. We note that the cut off frequency between these 2 noises is 600 seconds, this corresponds to the air-conditioning period. However we must establish the relationship between the Filcker noise and the temperature sensitivity to verify that the Flicker noise is due to the temperature variations. Even if the ZCDs sensitivity seems not to have an effect, it is necessary to fix this problem. Now we will explain how we can improve the obtained result with the appropriate processing.

3.4 Software

By working with a beat frequency of 1 KHz we can correct the VCO more often and keep the same performances with the appropriate processing as if we worked with a 1 Hz beat frequency. We have chosen to use the triangular averaging estimator to improve the ZCDs results. By making a measure with a triangular averaging estimator we can decrease the white phase noise effect without eliminating the frequency jumps or the phase jumps. We measure the beat frequencies with a 1 s gate and we shift this gate 1 ms every 1 ms during 1 second, thus we generate 1000 gates of 1 s, i.e. 1000 averages. Then we sum these gates in order to obtain the triangular averaging function of figure 5.

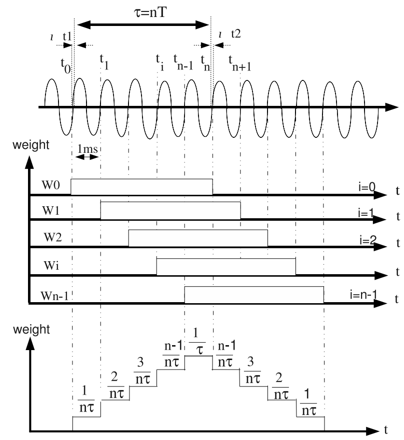

Figure 5: construction of triangular averaging estimator.

We choose to use this estimator because it is directly linked to the modified Allan estimator. On figure 6 we show the weight function of 2 triangular averages. W_m represents the triangular averaging weight function and W_{mvar} the modified Allan function. In fact if we have two triangular averaging functions shifted of τ the figure 6 and if we subtract these 2 functions: $-W_m(t) + W_m(t - \tau)$, we obtain the same function as the time sequence of the modified Allan deviation. Only the weight coefficient is different by a factor of $\sqrt{2}$. This principle is used in some counters [4]. It yields a $\tau^{-3/2}$ behaviour for the white phase noise and then decreases much more quickly than with the classical Allan variance (τ^{-1} behaviour).

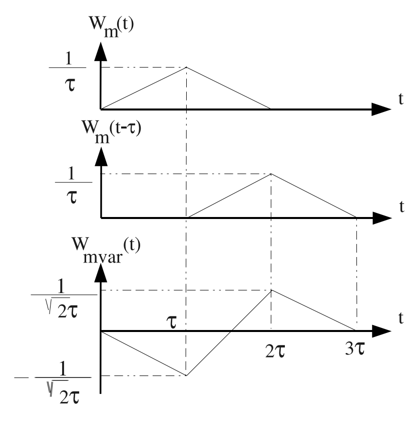

Figure 6: modified Allan function from 2 triangular averaging functions.

When we apply the triangular averaging estimator on the result of the test (grey curve fig. 4) we obtain the black curve on figure 4. After the heating time we obtain: $\sigma = 6\times10^{-11}$. If the signal were composed only of white phase noise (without Flicker noise nor temperature variation if it is independent) the σ would be better. However we obtain mod $\sigma_y(1s) = 6 \times 10^{-11}$ @ 1KHz so we can obtain:

$$\text{mod } \sigma_y(1s) = 6 \times 10^{-16} @100 \text{ MHz}.$$

4 Digital processing

4.1 Principle

The digital processing generates the correction signal needed by the VCO. This one is based on a virtual processing [5] composed of 2 loops (fig. 7). The first loop creates a signal where the maser (Hm) is controled by the cesium (Cs), then we use this signal in the second loop to control the VCO.

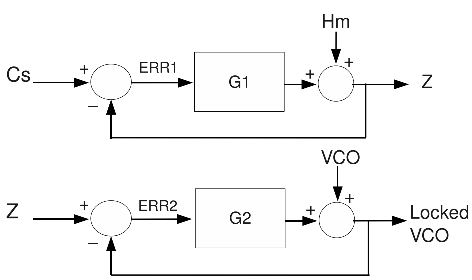

Figure 7: principle of virtual algorithm.

This principle allows to generate an output signal for the locked VCO (VCO_L) which depends on the free VCO (VCO_F), the maser (Hm) and the cesium (Cs); without modifying either the cesium or the maser.

$$VCO_L = VCO_F\frac{1+G1}{(1+G1)(1+G2)}+$$
$$Hm\frac{G2}{(1+G1)(1+G2)} + Cs\frac{G1G2}{(1+G1)(1+G2)}. \quad (1)$$

These 2 loops have the same transfer function but the time constants of G1 and G2 are different To generate the correction signal of the VCO we need the signal $ERR2$ (fig. 7). From the principle diagram we calculate $ERR2$ and obtain:

$$ERR2 = \frac{1}{(1+G1)(1+G2)}(Hm - VCO_F)+$$
$$\frac{G1}{(1+G1)(1+G2)}(Cs - VCO_F). \quad (2)$$

We note that it depends on 2 intercomparisons: $Hm - VCO_F$ and $Cs - VCO_F$. To create the transfer function of these 2 loops we use the Z transform and we create an infinite impulse response filter. With the Z transform the difference between the time constants does not appear that is why G1 =G2. But in the software, a k parameter allows to determine the correct cut off frequency of G2. We obtain the following transfer function:

$$G1 = \frac{Z^{-1} \times (b0 + b1 \times Z^{-1})}{(1-Z^{-1})^2}. \quad (3)$$

$$G1 = \frac{b0 \times Z^{-1} + b1 \times Z^{-2}}{1 - 2 \times Z^{-1} + Z^{-2}}. \quad (4)$$

We see that the transfer function depends on 2 parameters: $b0$ and $b1$. Thanks to Jury criteria we find 2 conditions on these parameters:

$$-2 < b1 < 0 \qquad \text{and} \qquad -b1 < b0 < 4.$$

By changing the parameters $b1$, $b0$ and k we modify the system stability.

4.2 Simulation

In order to validate the algorithm principle and find the best value of $b0$, $b1$ and k, we have done 2 simulation types. Firstly, to gain time we performed a non realistic simulation, where the cut off frequency between the VCO and the maser and the cut off frequency between the maser and the cesium was close, thus we fastly validated the algorithm principle. Now we work with realistic simulations, but the problem of these ones is that we must generate a file of about 160 G byte for obtaining a Allan deviation simulation with 10 decades. To see the behaviour of the locked VCO with the correct values for the VCO/maser cut off frequency and the cesium/maser cut off frequency, we need a simulation of 10 decades. The creation of this file requires about one week. On figure 8 we show the real Allan deviation simulation of the locked VCO.

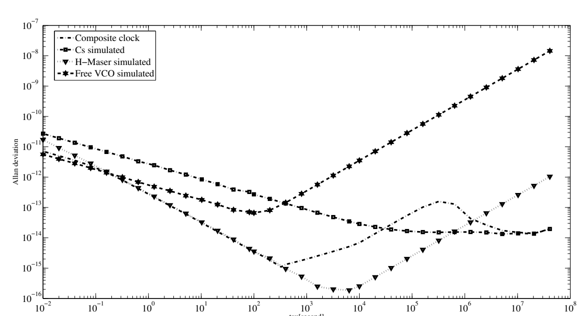

Figure 8: simulation of locked VCO

After many realistic or non realistic simulations we note that $b0$ and $b1$ modify the stability (convergence precision and speed) of the system and the cut off frequency between the maser and the VCO while k allows to find the correct maser/cesium cut off frequency. On figure 8 we see that the value of bo, $b1$, and k are not optimum. The control is good at the beginning, the locked VCO follows the free VCO then the maser. But afterwards the locked VCO tends to follow the cesium too early. To find the best value of $b0$, $b1$ and k for the best behaviour as possible we must perform many simulations, but we need a lot of time.

5 Digital to analog convertion

5.1 Principle

For the digital to analog conversion we have used a Digital to Analog Converter (DAC) with only 16 bits. We place a low pass filter with a constant time of about 1 s in DAC output and we generate an oversampling. In this way we can easily generate sublevels in one level of DAC, thus improving the precision of the command voltage of the VCO. In our case we use a VCO which works at 5 MHz with a tunning range of 2Hz for a command of 10V. So one level of DAC equals a variation of 31 μHz. For obtaining a relative instability of 5×10^{-13}@ 1ms, the maximun variation in VCO output must be of 2.5 μHz per millisecond. In order to obtain this stability we must generate 13 sublevels in one DAC level. We choose to create 16 sublevels in one DAC level. To perform one sublevel we change the DAC value between 2 succesive values, 2 times per millisecond. The moment where we change the DAC value between these 2 values determines the duty cycle. To generate 16 sublevels we must change 16 times the duty cycle between these 2 values. We can see this principle on figure 9.

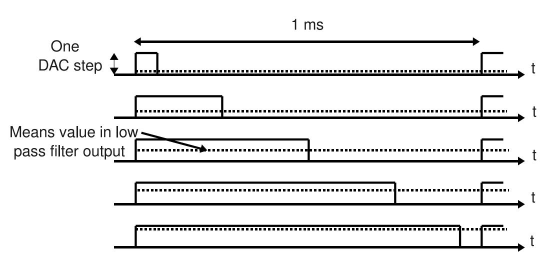

Figure 9: oversampling principle

The DAC value changes very fast compared to the constant time of the low pass filter, thus the output of this filter is a signal composed of little variations compared to the DAC level.

5.2 Simulation

We chose to generate 16 sublevels in one DAC level, thus we obtain a relative instability of 4×10^{-13} @ 1 ms. In order to verify that we do not degrade the stability we generated a simulation where the VCO is corrected every 1ms by sublevel which allows a relative stability of 5×10^{-13} (fig. 10). We note that even if we correct the VCO by sublevel, the locked VCO remains stable. The applied sublevels to the VCO do not alter this stability. Although the applied sublevels are very high compared to the free VCO variations, we notice no high variations in the locked VCO signal, the maximum variations correspond to a relative instability of 5×10^{-13}@ 1 ms.

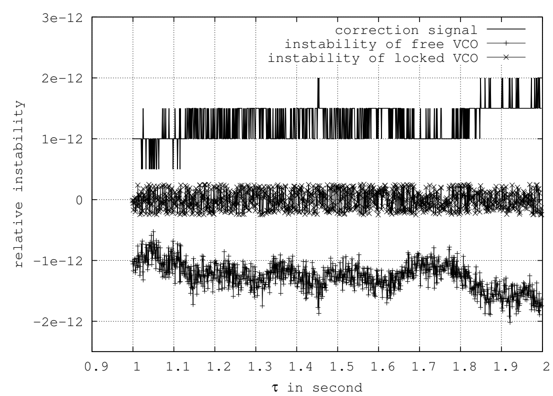

Figure 10: simulation of locked VCO

Now, we simulate on figure 11 the Allan deviation of the locked VCO generated previously on figure 10, for a triangular averaging estimator done with 100 and 1000 data. The first important point is the following: we do not degrade the stability of the VCO on the short term, the locked VCO keeps the stability of the free VCO even if we correct the VCO every millisecond by sublevel which corresponds to a relative instability of 5×10^{-13}. Secondly, we see the influence of the triangular averaging estimator on the Allan deviation. We note that the locked VCO follows the maser after 1s if we apply the triangular averaging on 1000 data, i.e. 1 sec. But when we do the triangular averaging on 100 values, i.e. 100 ms, we observe that the locked VCO follows more fastly the maser. We might think that it is more interesting to use the moving averaging on only 100 data but we must not forget that the measurement of signals, which come from the ZCDs, use this triangular averaging in order to decrease the white phase noise effect. So if we use the triangular averaging on 100 data, the white phase noise effect will be higher than if we use the triangular averaging on 1000 data. If the ZCD results are sufficient to use the triangular averaging with only 100 data, it is also the best choice. We will choose the number of data after having assembled the system and having done many tests. The advantage of this digital to analog convertion is that we can improve the relative instability only by changing the software. In fact, to improve the stability we need to increase the number of sublevels, and we can do it only by changing the software, we do not need to change the hardware. The maximal number of sublevels depends on the maximal speed necessary for the DAC to change its value.

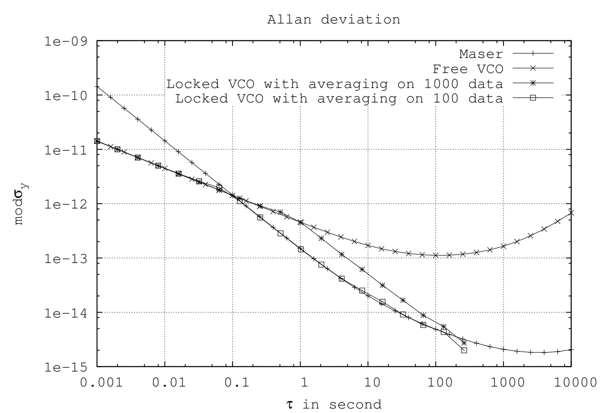

Figure 11: simulation of Allan deviation of locked VCO

We do many test where we control the VCO with this principle and we can confirm that we do not degrade the VCO stability on the short term and we can obtain a relative instability better than 1×10^{-15} after 1s, but we must program the software for the global system.

6 Conclusion

Even if we must do again many tests we notice that the principle of the composite clock is approved and the obtained results are encouraging. The obtained results on the short term are sufficient to use the ZCDs. We can obtain mod$\sigma_y(1s)$ lower than 1×10^{-15} but we must fix the problem concerning the temperature sensitivity of the ZCDs. From other tests we deduce that we cannot use the ZCDs in this project if we do not decrease or eliminate the temperature sensitivity of the ZCDs. However we think that they come from either the power supply variations or the phase variations of the first 2 amplifier stages of the ZCDs, which have a low passs filter. If the sensitivity comes from the phase variation, then we will have to increase the bandwidth in order to move the signal frequency (1 KHz) away from the cut off frequency of the low pass filter, but we will increase the noise. Even if we increase the noise, the ZCDs noise are sufficiently low on the short term not to alter the stability of the output signal. Concerning the digital processing the biggest problem is the time needed to generate a real simulation, but the principle is validated. We must find the best value for bo, $b1$, and k then implement the program in the PC. The digital to analog conversion is correct, the tests that we did prove it. Now we must program the necessary software for the VCO when it will be locked. To conclude we must fix the ZCDs sensitivity to the temperature before assembling the different parts of the system and program the software of digital to analog convertion. This system should allow us to create a composite clock which should have the longest stability range.

References

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